### IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:

KAWAMA, Shuichi et al

Appl. No.:

NEW

Group:

Filed:

March 18, 2004

Examiner:

For:

SWITCHED CAPACITOR FILTER AND DIGITAL

WIRELESS RECEIVER

INFORMATION DISCLOSURE STATEMENT (SUBMISSION CONCURRENT WITH THE FILING OF A NEW PATENT APPLICATION)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

March 18, 2004

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

### I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

# II. COPIES

- a. This application was filed before June 30, 2003.

  Accordingly, submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.
- b. A This application was filed on or after June 30, 2003. Accordingly, copies of cited US patents and patent application publications therefore are not included. Copies of foreign patent documents and non-patent literature are included.

c. 
This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should be forwarded from the International Search Authority. If copies are needed, please contact the undersigned.

# III. CONCISE EXPLANATION OF THE RELEVANCE (check at least one box)

# a. DOCUMENTS IN THE ENGLISH LANGUAGE

The patents, publications, or other information listed on the attached PTO 1449 are in the English language and therefore, do not require a statement of relevancy.

# b. DOCUMENTS NOT IN THE ENGLISH LANGUAGE

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

The relevancy of the Japanese language document can be determined from a review of the English language Abtract and Partial Translation attached thereto.

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An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

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The following additional information is provided for the Examiner's consideration.

#### FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By

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TCB/smt 1248-0704P Falls Church, VA 22040-0747

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Attachment(s):	$\boxtimes$	Form PTO-1449(s)		
	$\boxtimes$	Documents		

☐ Foreign Search Report

☐ Fee

Other:

(Rev. 02/12/2004)

Form PTO-1449				ATTY. DOCKET NO. 1248-0704P	APPLICATION NO. NEW						
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OTHER journal, ser	DOCUI	MENTS (Include Namum, catalog, etc.) date	me of the autho	r (in CAPITAL LETTERS), me-issue number(s), publ	title of the article (when appr isher, city and/or country when	opriate), tit e published.	tle of the it	em (book, i	magasine,		
	Azuma et al., IEEE Journal of Solid-State Circuits, Vol. 37, No. 3 March 2002 pages 349-356										
	Azuma et al., 2004 IEEE International Solid-State Circuit conference, pages 1-3										
	Sender	owicz et al.,	IEEE 200	1							
	Hsieh et al., IEEE Journal of Solid-State Circuit, Vol. SC-16, No. 6, December 1981 pages 708-715										
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